AKAI

# HOME THEATER SYSTEM

Model:
HT-A-1150

# SERVICE MANUAL

www.akai.ru

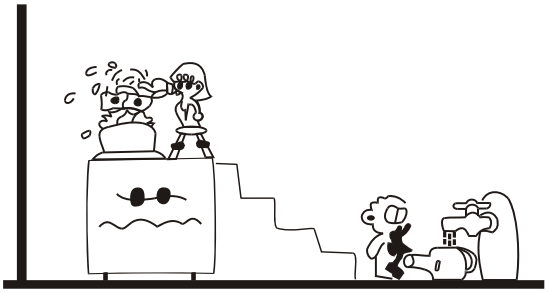
# CONTENTS

# 1. SAFETY PRECAUTIONS

***PRECAUTIONS:***

1. **Power supply:** This speaker can only use the type of power supply as specified in the instruction manual or marked on the master speaker.

2. **Power line protection:** Make sure to avoid power line being trampled, pulled or squeezed by heavy objects. In particular, be sure to hold the plug when pulling the power line from the socket. Never pull on the power line. besides, keep the power line away from hot objects.

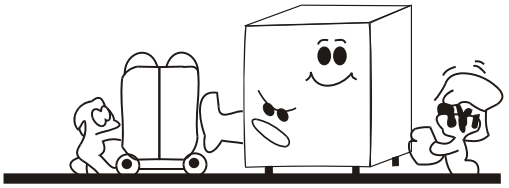


3. **Cord polarity:** The speaker cord must be correctly connected as per marking on the function panel."+" and "–" Must have correct polarity so maximize the inherent quality of the speaker. Otherwise, normal function and output will be affected.

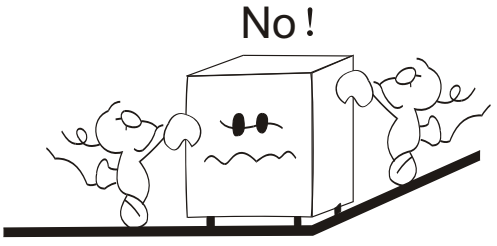
4. **Ventilation:** This speaker has good adaptability to the environment, but pay attention to the environmental ventilation during long periods of work.

5. **Water and moisture:** Keep the sound box away from rain, water spray, water splash and wet environment, such as bath, kitchen, water basin, washing basin, damp basement, swimming pool, etc.

6. **Removing cabinet:** In case of speaker failure or problems due to improper use, don't dismantle the unit to repair or check by yourself. Please turn off the power and use after checked by specialists to avoid causing personal accident.



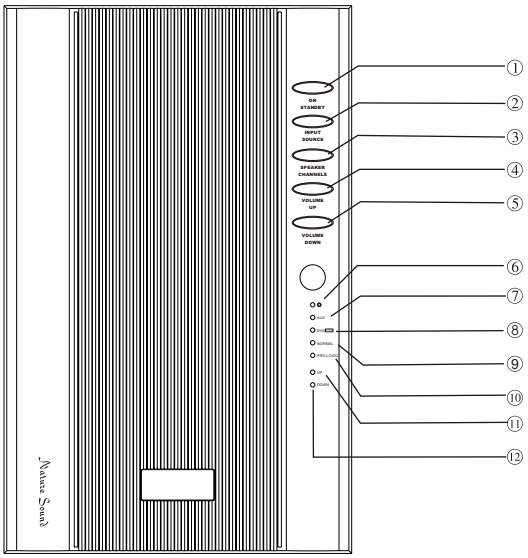
7. **Appearance cleaning:** Don't use volatile solutions to clean the speaker to avoid damaging the appearance.




8. **Please cut off the power:** If you don't use the sound system for a long time, please remove the cable wire or disconnect the power to ensure the speaker safety and household safety.

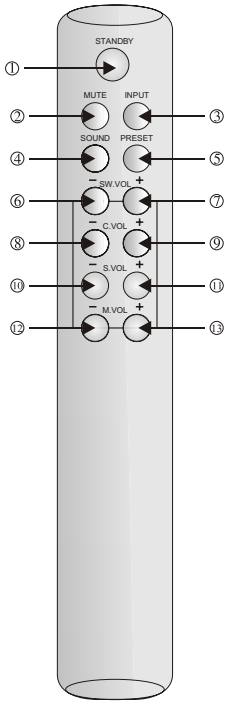
# 2. LOCATION OF USERS CONTROLS

## *FRONT PANEL INSTRUCTION :*



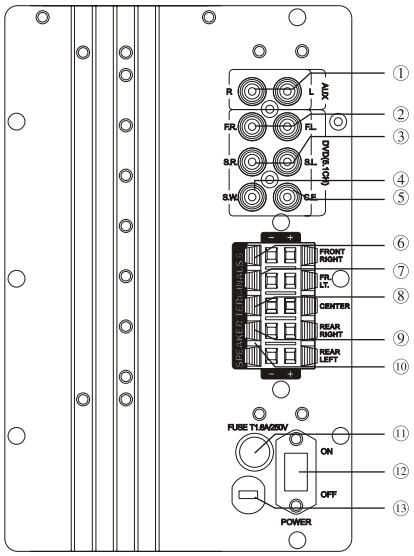

| | | | |
|---|---|---|---|
| ON STANDBY | ① Power switch button(standby) switch on or off for waiting or on condition | INPUT SOURCE | ② Signal input selection |
| SPEAKER CHANNELS | ③ Sound field selection | VOLUME UP | ④ Master volume in increase selection |
| VOLUME DOWN | ⑤ Master volume decrease selection | ○ | ⑥ Working /standby indicator |
| AUX | ⑦ AUX signal input indicator | DVD | ⑧ DVD signal input indicator |
| NORMAL | ⑨ NORMAL sound field indicator | PRO.LOGIC | ⑩ Pro.logic sound field indicator |
| UP | ⑪ Volume increase indicator | DOWN | ⑫ Volume decrease indicator |

## *REMOTE CONTROL INSTRUCTION :*




| | |
|---|---|
| ① | Working/stanby |
| ② | mute button |
| ③ | input signal button |
| ④ | Sound field select |
| ⑤ | preset button |
| ⑥ | bass volume down |
| ⑦ | bass volume up |
| ⑧ | center volume down |
| ⑨ | center volume up |
| ⑩ | surround volume down |
| ⑪ | surround volume up |
| ⑫ | main volume down |
| ⑬ | main volume up |

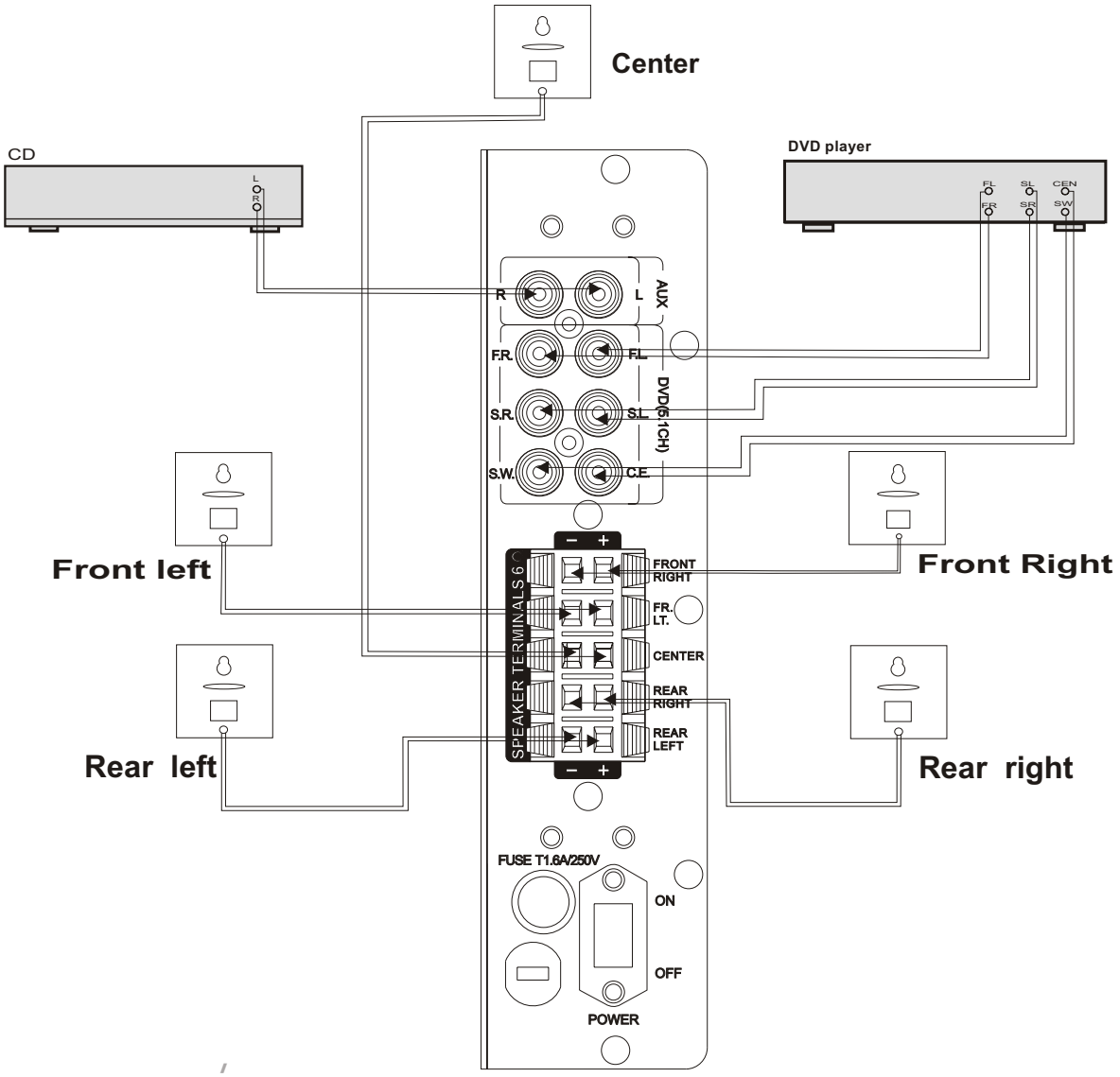
## *BACK PANEL DESCRIPTION:*




| | |
|---|---|
| ① AUX L/R INPUT | ② DVD F.R./F.L.INPUT |
| ③ DVD S.R./S.L.INPUT | ④ DVD S.W.INPUT |
| ⑤ DVD C.E.INPUT | ⑥ SPEAKER OUTPUT F.R. |
| ⑦ SPEAKER OUTPUT F.L. | ⑧ SPEAKER OUTPUT C.E. |
| ⑨ SPEAKER OUTPUT S.R. | ⑩ SPEAKER OUTPUT S.L. |
| ⑪ FUSE T1.6A/250V | ⑫ POWER SWITCH |
| ⑬ POWER | |

# 3. CONNECTING TO EQUIPMENT

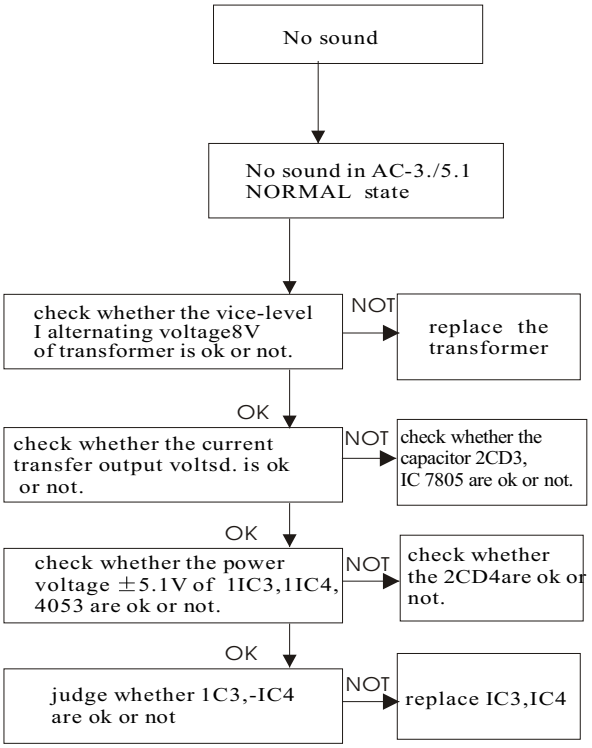
## *SYSTEM CONNECTION:*



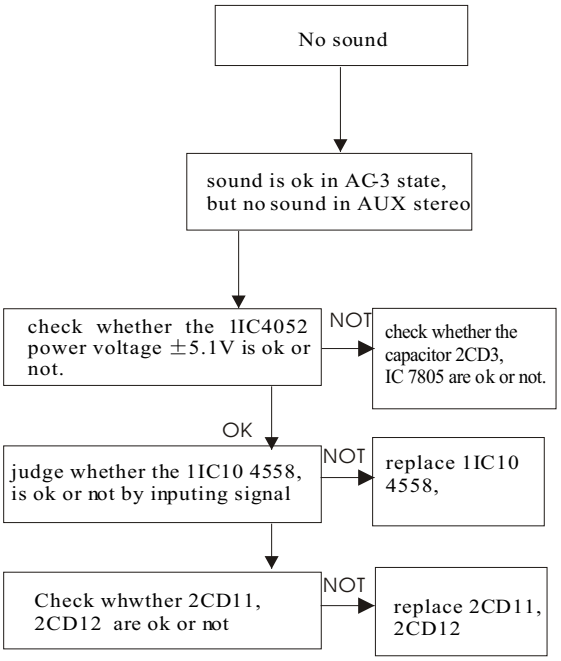
# 4. TROUBLE SHOOTING GUIDE

***TROUBLE SHOOTING AND RESOLUTION***

**1**



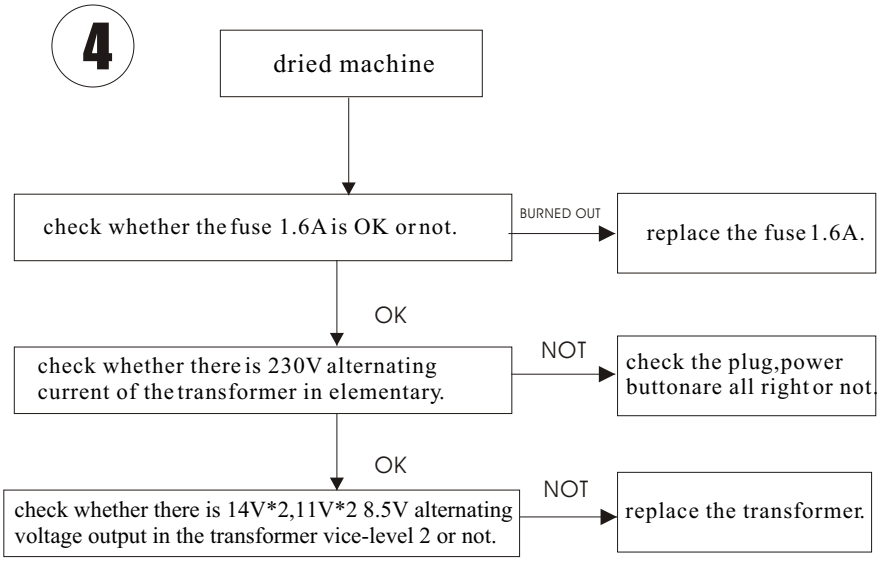

**2**



# 4. TROUBLE SHOOTING GUIDE

***TROUBLE SHOOTING AND RESOLUTION***

**4**




**5**

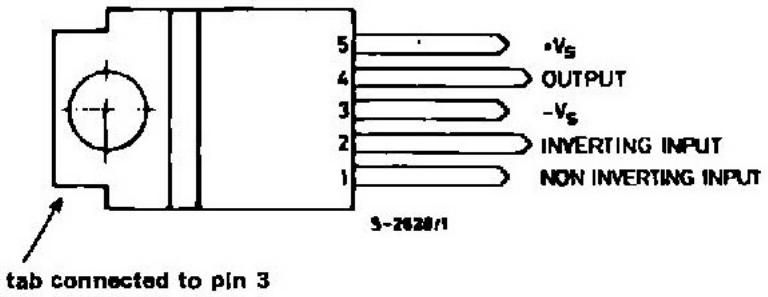
| Error | Possible reason | Obivating |
|---|---|---|
| No sound | The power plug is not exactly inserted.<br>The connection of output and input is not well<br>The input format is not right<br>The volume control be settled in the minimum<br>Rest estate | Insert the plug in right place<br>Connect the output and input cables<br>Adjust the volume |

# 5. INTERNAL BLOCK DIAGRAM OF ICS

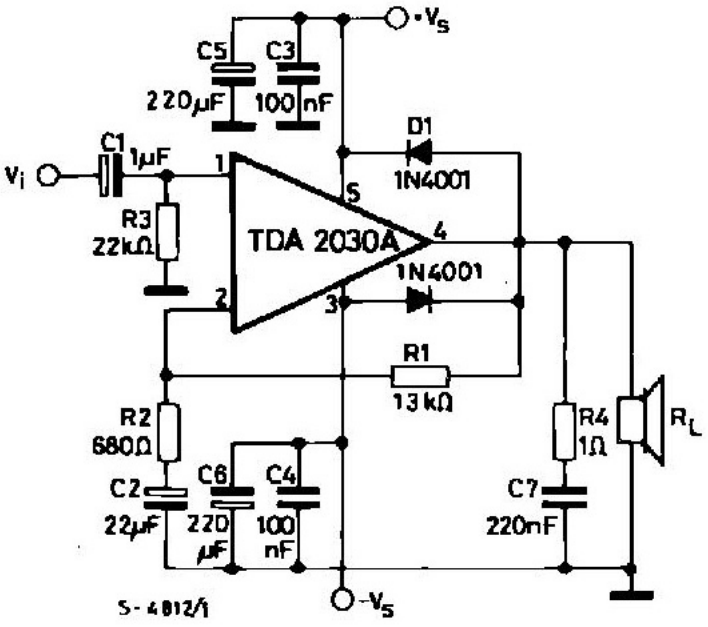
## TDA2030A

### TDA2030A

**PIN CONNECTION** (Top view)




**TEST CIRCUIT**



# 5. INTERNAL BLOCK DIAGRAM OF ICS



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_s$ | Supply Voltage | ± 22 | V |
| $V_i$ | Input Voltage | $V_s$ | |
| $V_i$ | Differential Input Voltage | ± 15 | V |
| $I_o$ | Peak Output Current (internally limited) | 3.5 | A |
| $P_{tot}$ | Total Power Dissipation at $T_{case}$ = 90 °C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and Junction Temperature | – 40 to + 150 | °C |

## ELECTRICAL CHARACTERISTICS

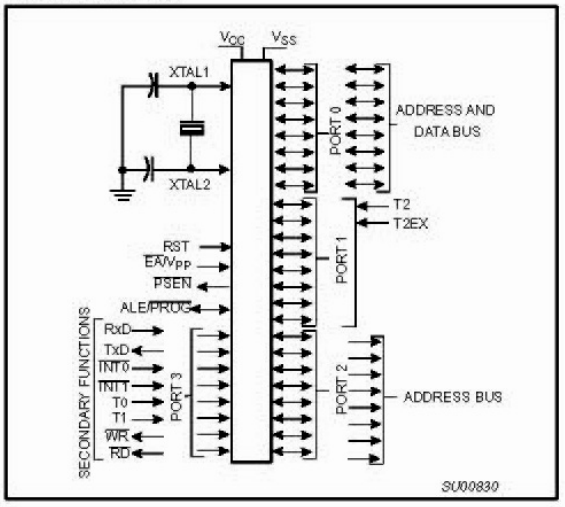
(Refer to the test circuit, $V_S$ = ± 16V, $T_{amb}$ = 25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply Voltage | | ± 6 | | ± 22 | V |
| $I_d$ | Quiescent Drain Current | | | 50 | 80 | mA |
| $I_b$ | Input Bias Current | $V_S$ = ± 22V | | 0.2 | 2 | µA |
| $V_{os}$ | Input Offset Voltage | $V_S$ = ± 22V | | ± 2 | ± 20 | mV |
| $I_{os}$ | Input Offset Current | | | ± 20 | ± 200 | nA |
| $P_O$ | Output Power | d = 0.5%, $G_v$ = 26dB, f = 40 to 15000Hz<br>$R_L$ = 4Ω<br>$R_L$ = 8Ω<br>$V_S$ = ± 19V, $R_L$ = 8Ω | <br>15<br>10<br>13 | <br>18<br>12<br>16 | | W |
| BW | Power Bandwidth | $P_o$ = 15W, $R_L$ = 4Ω | | 100 | | kHz |
| SR | Slew Rate | | | 8 | | V/µsec |
| $G_v$ | Open Loop Voltage Gain | f = 1kHz | | 80 | | dB |
| $G_v$ | Closed Loop Voltage Gain | f = 1kHz | 25.5 | 26 | 26.5 | dB |
| d | Total Harmonic Distortion | $P_o$ = 0.1 to 14W, $R_L$ = 4Ω, f = 40 to 15 000Hz<br>f = 1kHz<br>$P_o$ = 0.1 to 9W, f = 40 to 15 000Hz, $R_L$ = 8Ω | | 0.08<br>0.03<br>0.5 | | %<br>%<br>% |
| $d_2$ | Second Order CCIF Intermodulation Distortion | $P_O$ = 4W, $f_2 - f_1$ = 1kHz, $R_L$ = 4Ω | | 0.03 | | % |
| $d_3$ | Third Order CCIF Intermodulation Distortion | $f_1$ = 14kHz, $f_2$ = 15kHz, $2f_1 - f_2$ = 13kHz | | 0.08 | | % |
| $e_N$ | Input Noise Voltage | B = Curve A<br>B = 22Hz to 22kHz | | 2<br>3 | <br>10 | µV<br>µV |
| $i_N$ | Input Noise Current | B = Curve A<br>B = 22Hz to 22kHz | | 50<br>80 | <br>200 | pA<br>pA |
| S/N | Signal to Noise Ratio | $R_L$ = 4Ω, $R_g$ = 10kΩ, B = Curve A<br>$P_O$ = 15W<br>$P_O$ = 1W | | <br>106<br>94 | | <br>dB<br>dB |
| $R_i$ | Input Resistance (pin 1) | (open loop) f = 1kHz | 0.5 | 5 | | MΩ |
| SVR | Supply Voltage Rejection | $R_L$ = 4Ω, $R_g$ = 22kΩ, $G_v$ = 26dB, f = 100 Hz | | 54 | | dB |
| $T_j$ | Thermal Shut-down Junction Temperature | | | 145 | | °C |

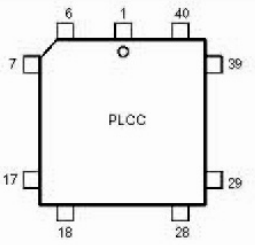
# 5. INTERNAL BLOCK DIAGRAM OF ICS

## 89C52

### LOGIC SYMBOL




### PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

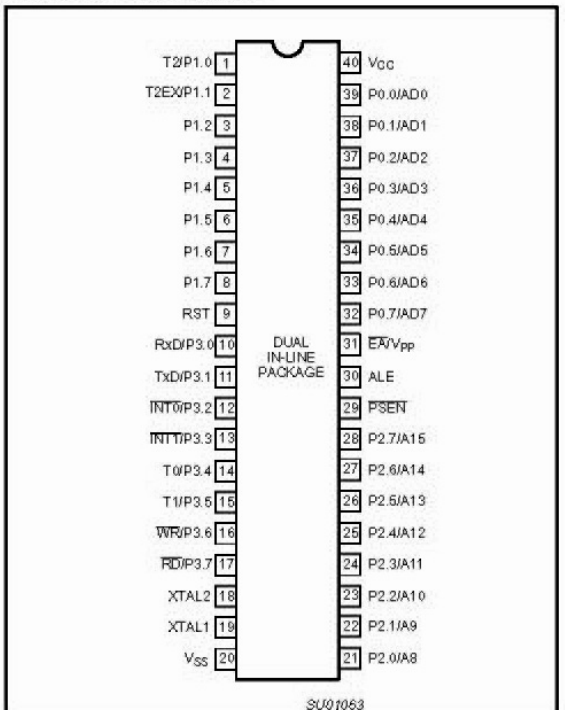



| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NIC* | 16 | P3.4/T0 | 31 | P2.7/A15 |
| 2 | P1.0/T2 | 17 | P3.5/T1 | 32 | PSEN |
| 3 | P1.1/T2EX | 18 | P3.6/WR | 33 | ALE |
| 4 | P1.2 | 19 | P3.7/RD | 34 | NIC* |
| 5 | P1.3 | 20 | XTAL2 | 35 | EA/VPP |
| 6 | P1.4 | 21 | XTAL1 | 36 | P0.7/AD7 |
| 7 | P1.5 | 22 | VSS | 37 | P0.6/AD6 |
| 8 | P1.6 | 23 | NIC* | 38 | P0.5/AD5 |
| 9 | P1.7 | 24 | P2.0/A8 | 39 | P0.4/AD4 |
| 10 | RST | 25 | P2.1/A9 | 40 | P0.3/AD3 |
| 11 | P3.0/RxD | 26 | P2.2/A10 | 41 | P0.2/AD2 |
| 12 | NIC* | 27 | P2.3/A11 | 42 | P0.1/AD1 |
| 13 | P3.1/TxD | 28 | P2.4/A12 | 43 | P0.0/AD0 |
| 14 | P3.2/INT0 | 29 | P2.5/A13 | 44 | VCC |
| 15 | P3.3/INT1 | 30 | P2.6/A14 | | |

* NO INTERNAL CONNECTION

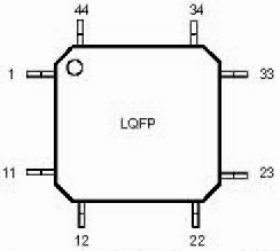
SU01062

### PLASTIC DUAL IN-LINE PACKAGE PIN CONFIGURATIONS




SU01063

### LOW PROFILE QUAD FLAT PACK PIN FUNCTIONS




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | P1.5 | 16 | VSS | 31 | P0.6/AD6 |
| 2 | P1.6 | 17 | NIC* | 32 | P0.5/AD5 |
| 3 | P1.7 | 18 | P2.0/A8 | 33 | P0.4/AD4 |
| 4 | RST | 19 | P2.1/A9 | 34 | P0.3/AD3 |
| 5 | P3.0/RxD | 20 | P2.2/A10 | 35 | P0.2/AD2 |
| 6 | NIC* | 21 | P2.3/A11 | 36 | P0.1/AD1 |
| 7 | P3.1/TxD | 22 | P2.4/A12 | 37 | P0.0/AD0 |
| 8 | P3.2/INT0 | 23 | P2.5/A13 | 38 | VCC |
| 9 | P3.3/INT1 | 24 | P2.6/A14 | 39 | NIC* |
| 10 | P3.4/T0 | 25 | P2.7/A15 | 40 | P1.0/T2 |
| 11 | P3.5/T1 | 26 | PSEN | 41 | P1.1/T2EX |
| 12 | P3.6/WR | 27 | ALE | 42 | P1.2 |
| 13 | P3.7/RD | 28 | NIC* | 43 | P1.3 |
| 14 | XTAL2 | 29 | EA/VPP | 44 | P1.4 |
| 15 | XTAL1 | 30 | P0.7/AD7 | | |

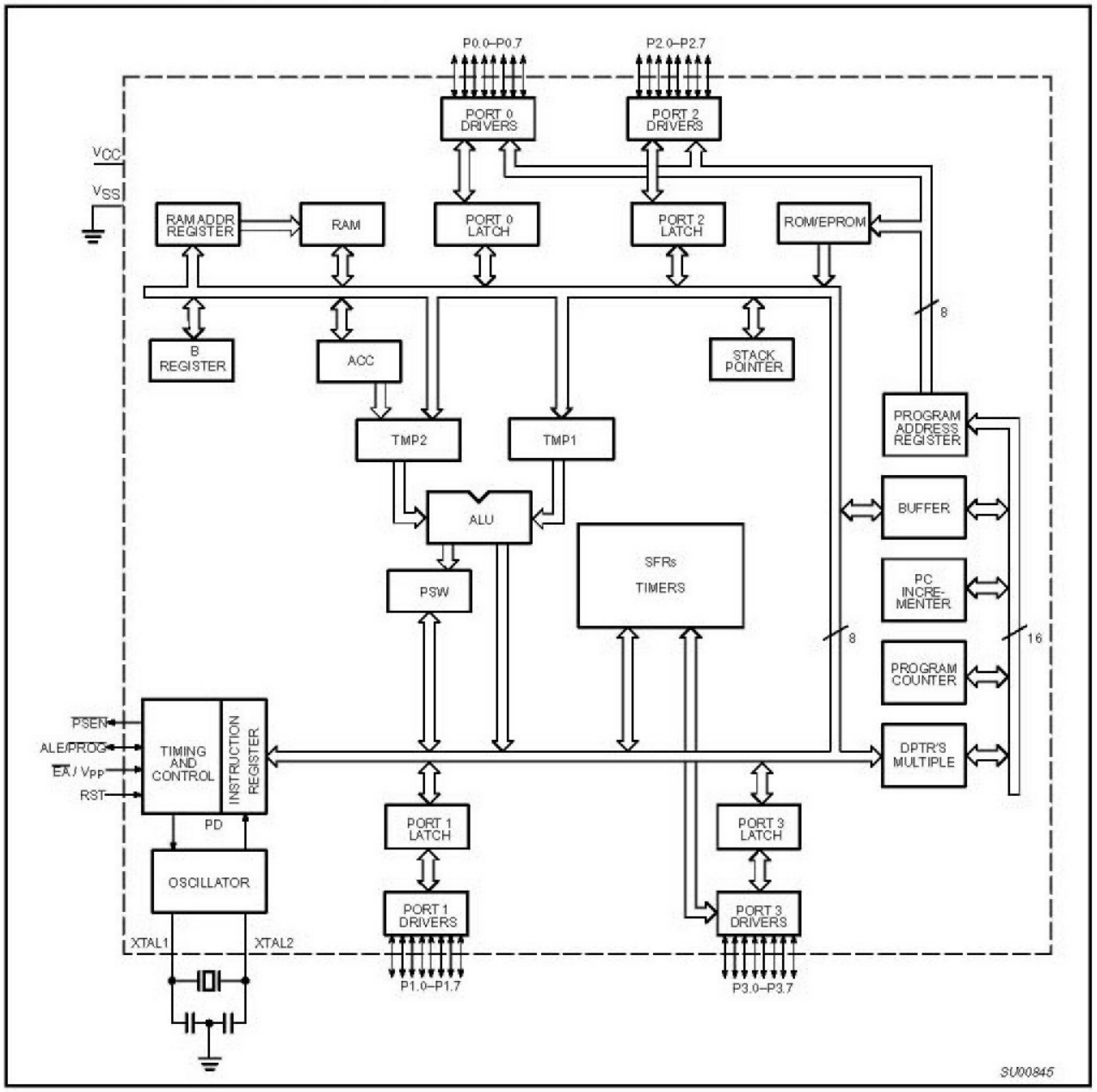
* NO INTERNAL CONNECTION

SU01487

# 5. INTERNAL BLOCK DIAGRAM OF ICS

## 89C52

**BLOCK DIAGRAM 2 (CPU-ORIENTED)**



# 5. INTERNAL BLOCK DIAGRAM OF ICS

## 89C52

**PIN DESCRIPTIONS**

| MNEMONIC | PIN NUMBER DIP | PLCC | LQFP | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|
| $V_{SS}$ | 20 | 22 | 16 | I | **Ground:** 0 V reference. |
| $V_{CC}$ | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for normal, idle, and power-down operation. |
| P0.0-0.7 | 39–32 | 43–36 | 37–30 | I/O | **Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during Flash programming. External pull-ups are required during program verification. |
| P1.0–P1.7 | 1–8 | 2–9 | 40–44, 1–3 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: $I_{IL}$). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include: |
| | 1 | 2 | 40 | I/O | **T2 (P1.0):** Timer/Counter 2 external count input/clockout (see Programmable Clock-Out) |
| | 2 | 3 | 41 | I | **T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction control |
| P2.0–P2.7 | 21–28 | 24–31 | 18–25 | I/O | **Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: $I_{IL}$). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during Flash programming and verification. |
| P3.0–P3.7 | 10–17 | 11, 13–19 | 5, 7–13 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: $I_{IL}$). Port 3 also serves the special features of the 80C51 family, as listed below: |
| | 10 | 11 | 5 | I | **RxD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TxD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{INT0}$ (P3.2):** External interrupt |
| | 13 | 15 | 9 | I | **$\overline{INT1}$ (P3.3):** External interrupt |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input |
| | 16 | 18 | 12 | O | **$\overline{WR}$ (P3.6):** External data memory write strobe |
| | 17 | 19 | 13 | O | **$\overline{RD}$ (P3.7):** External data memory read strobe |
| RST | 9 | 10 | 4 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$. |
| ALE/$\overline{PROG}$ | 30 | 33 | 27 | O | **Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (12-clk) or 1/3 (6-clk Mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction. |
| $\overline{PSEN}$ | 29 | 32 | 26 | O | **Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. |
| $\overline{EA}$/$V_{PP}$ | 31 | 35 | 29 | I | **External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH/1FFFH/3FFFH/7FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than the on-chip Flash. This pin also receives the 5 V / 12 V programming supply voltage ($V_{PP}$) during Flash programming. If security bit 1 is programmed, $\overline{EA}$ will be internally latched on Reset. |
| XTAL1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier. |

**NOTE:**
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than $V_{CC}$ + 0.5 V or $V_{SS}$ – 0.5 V, respectively.

# CD4053B

## *CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion*

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to $20V_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if $V_{DD}$-$V_{SS}$ = 3V, a $V_{DD}$-$V_{EE}$ of up to 13V can be controlled; for $V_{DD}$-$V_{EE}$ level differences above 13V, a $V_{DD}$-$V_{SS}$ of at least 4.5V is required). For example, if $V_{DD}$ = +4.5V, $V_{SS}$ = 0V, and $V_{EE}$ = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}$-$V_{SS}$ and $V_{DD}$-$V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic Ò1Ó is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw conÞguration.

When these devices are used as demultiplexers, the ÒCHANNEL IN/OUTÓ terminals are the outputs and the ÒCOMMON OUT/INÓ terminals are the inputs.

## *Ordering Information*

| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE |
|---|---|---|
| CD4051BF, CD4052BF, CD4053BF | -55 to 125 | 16 Ld CERAMIC DIP |
| CD4051BE, CD4052BE, CD4053BE | -55 to 125 | 16 Ld PDIP |
| CD4051BM, CD4061BNS | -55 to 125 | 16 Ld SOIC |
| CD4051BPW, CD4052BPW, CD4053BPW | -55 to 125 | 16 Ld TSSOP |

## *Features*

- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . ≤$20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for $V_{DD}$-$V_{EE}$ = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at $V_{DD}$-$V_{EE}$ = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V ($V_{DD}$-$V_{SS}$ = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ ($V_{DD}$-$V_{EE}$ = 20V)
- Matched Switch Characteristics, $r_{ON}$ = 5Ω (Typ) for $V_{DD}$-$V_{EE}$ = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at $V_{DD}$-$V_{SS}$ = $V_{DD}$-$V_{EE}$ = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25$^{O}$C
- Break-Before-Make Switching Eliminates Channel Overlap

## *Applications*

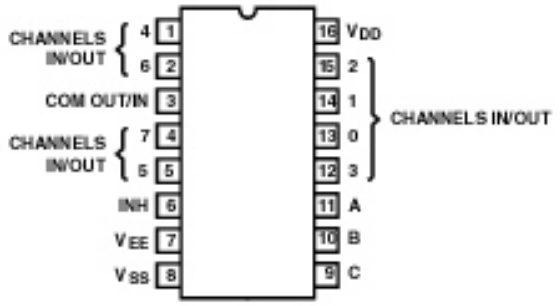
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

# 5. INTERNAL BLOCK DIAGRAM OF ICS

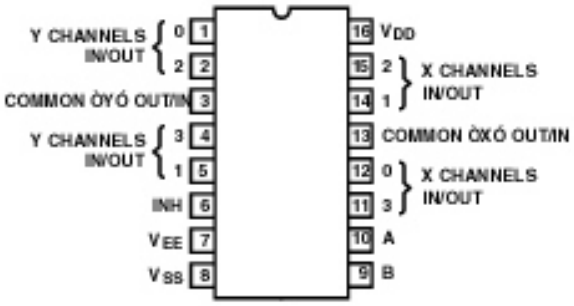
## CD4053B

### *Pinouts*

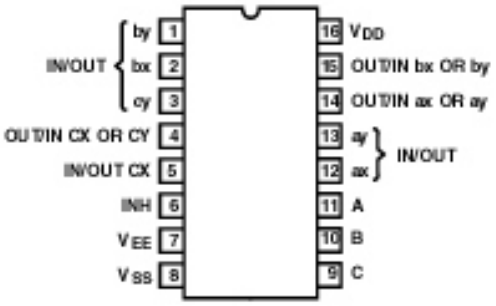
CD4051B (PDIP, CDIP, SOIC, TSSOP)
TOP VIEW



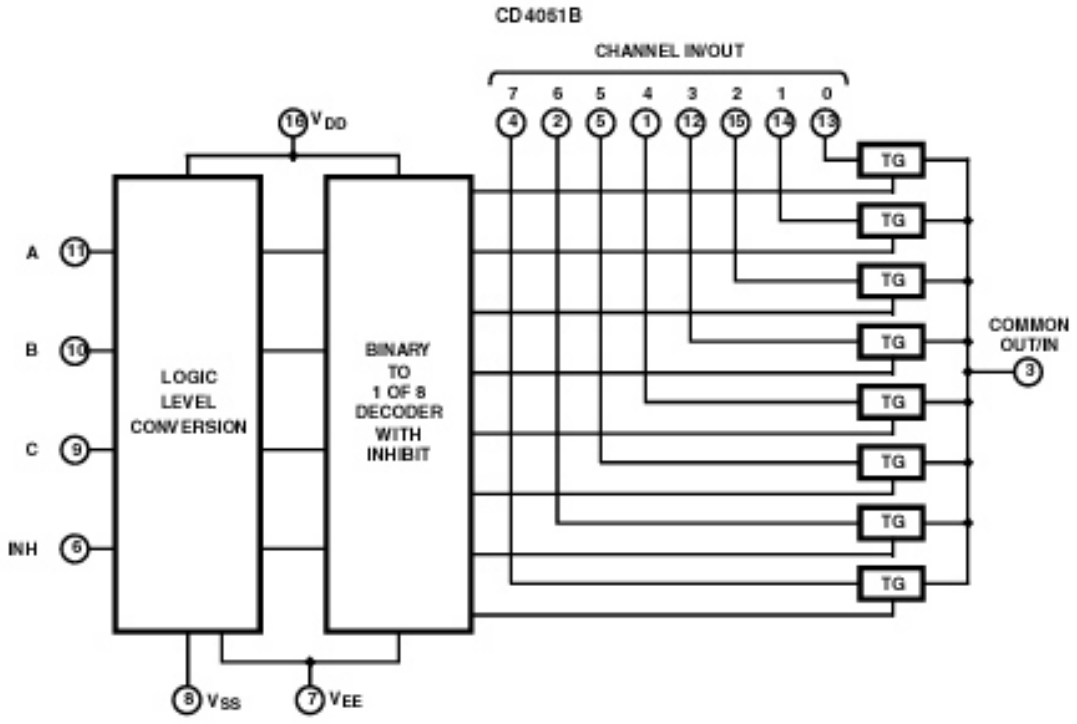

CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW




CD4053B (PDIP, CDIP, TSSOP)
TOP VIEW




### *Functional Block Diagrams*

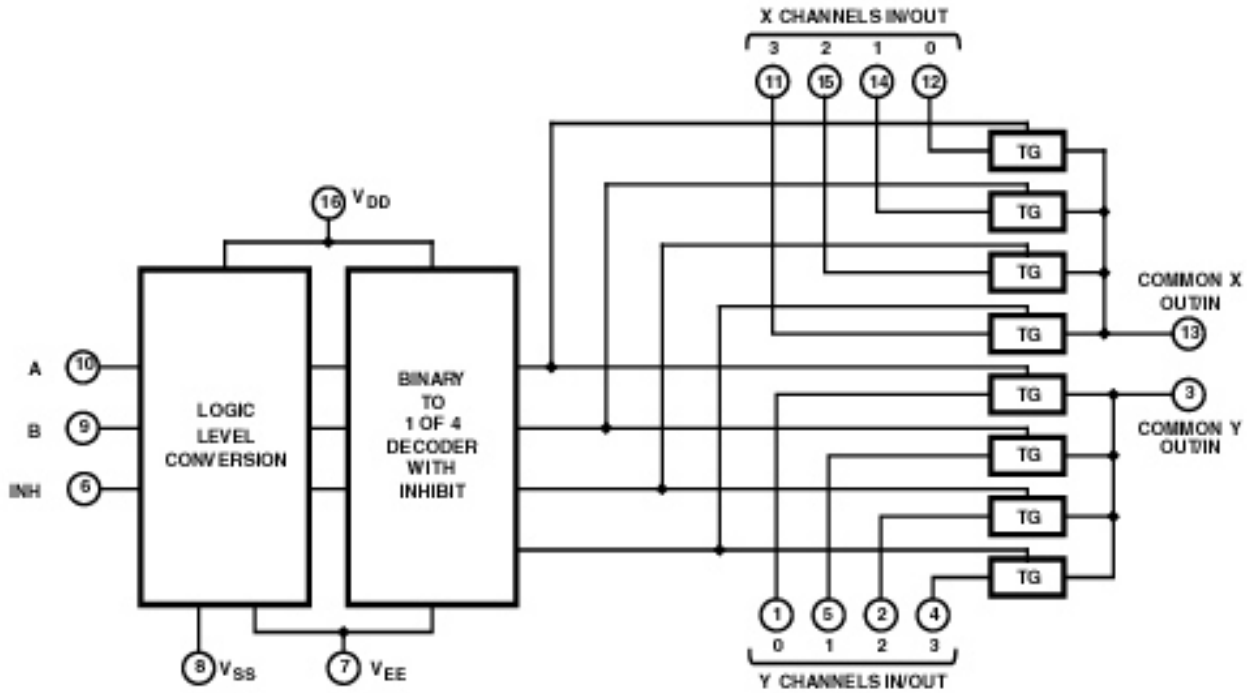



All inputs are protected by standard CMOS protection network.

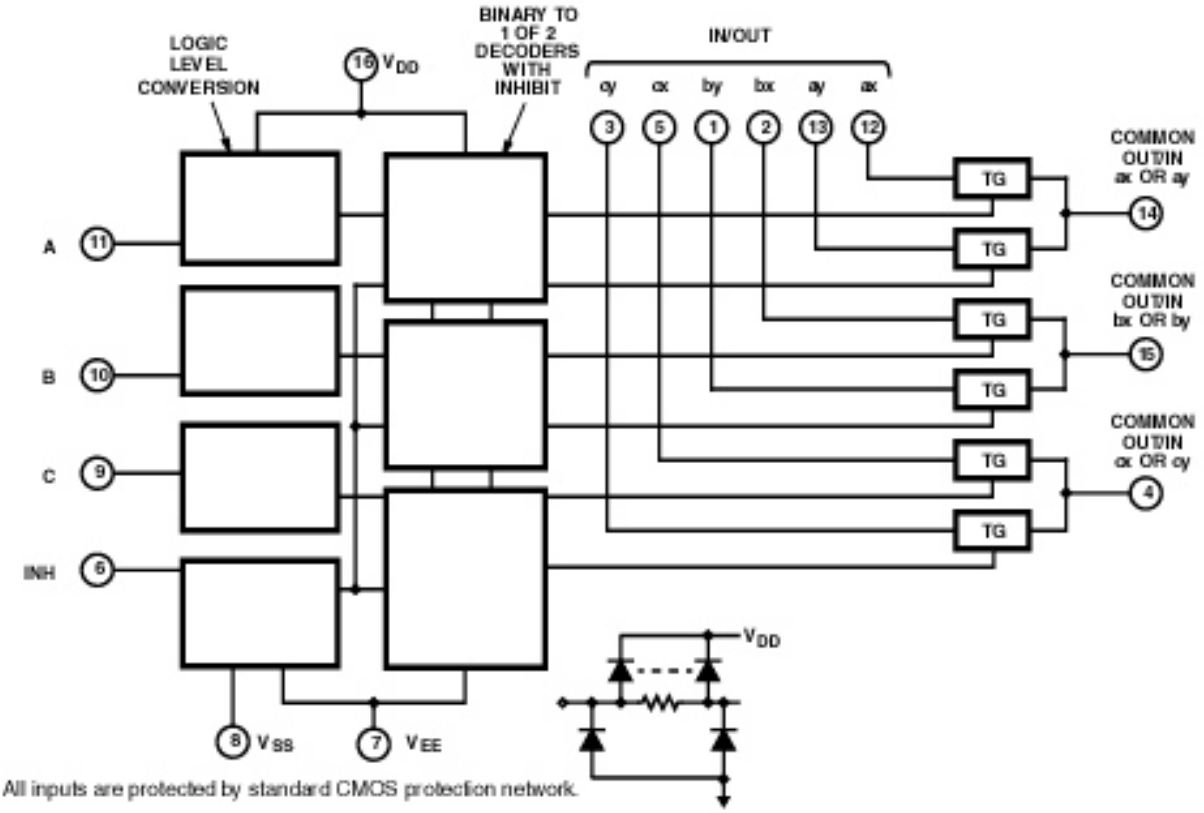
# CD4053B

***Functional Block Diagrams*** (Continued)

CD4052B




CD4053B



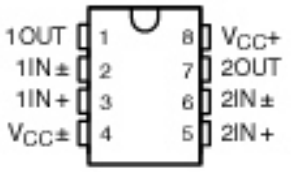

All inputs are protected by standard CMOS protection network.

# JRC 4558

SLOS073A ± MARCH 1976 ± REVISED JUNE 1999

- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth . . . 3 MHz Typ
- Gain and Phase Match Between Amplifiers
- Low Noise . . . 8 nV/$\sqrt{\text{Hz}}$ Typ at 1 kHz
- Designed To Be Interchangeable With Raytheon RC4558 and RM4558 Devices

D, JG, P, OR PS PACKAGE
(TOP VIEW)




## description

The RC4558 and RM4558 devices are dual general-purpose operational amplifiers with each half electrically similar to the µA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RC4558 is characterized for operation from 0°C to 70°C, and the RM4558 is characterized for operation over the full military temperature range of ±55°C to 125°C.

AVAILABLE OPTIONS

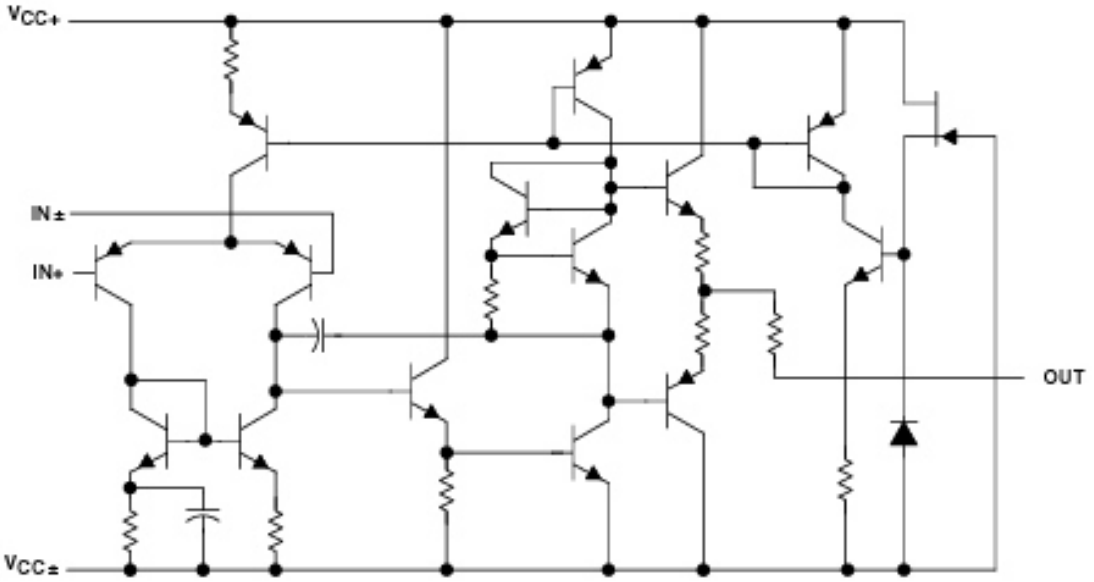
| $T_A$ | $V_{IO}$MAX AT 25°C | PACKAGED DEVICES | | | | |
|---|---|---|---|---|---|---|
| | | SMALL OUTLINE (D) | SSOP (DBR) | CERAMIC DIP (JG) | PLASTIC DIP (P) | SOP (PSR) |
| 0°C to 70°C | 6 mV | RC4558D | RC4558DBR | Ð | RC4558P | RC4558PSR |
| ±55°C to 125°C | 6 mV | Ð | Ð | RM4558JG | Ð | Ð |

The D package is available taped and reeled. Add the suffix R to the device type (e.g., RC4558DR).

# JRC 4558

SLOS073A ± MARCH 1976 ± REVISED JUNE 1999

## schematic (each amplifier)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | RC4558 | RM4558 | UNIT |
|---|---|---|---|---|
| Supply voltage (see Note 1) | $V_{CC+}$ | 18 | 22 | V |
| | $V_{CC\pm}$ | ±18 | ±22 | |
| Differential input voltage (see Note 2) | | ±30 | ±30 | V |
| Input voltage (any input, see Notes 1 and 3) | | ±15 | ±15 | V |
| Duration of output short circuit to ground, one amplifier at a time (see Note 4) | | unlimited | unlimited | |
| Package thermal impedance, $\theta_{JA}$ (see Note 5) | D package | 197 | | °C/W |
| | P package | 104 | | |
| | PS package | 163 | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package | | | 300 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package | | 260 | | °C |
| Storage temperature range, $T_{stg}$ | | ±65 to 150 | ±65 to 150 | °C |

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between $V_{CC+}$ and $V_{CC\pm}$.
2. Differential voltages are at IN+ with respect to IN±.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

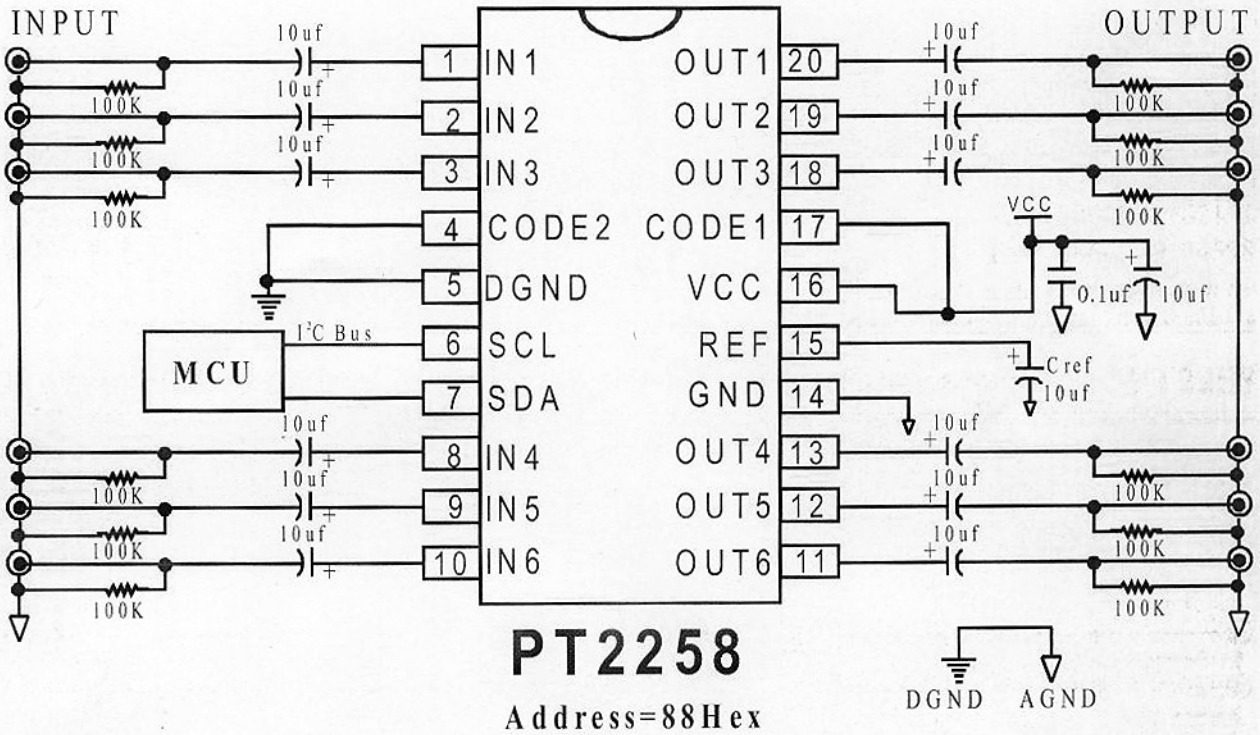
## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{CC+}$ | 5 | 15 | V |
| | $V_{CC\pm}$ | ±5 | ±15 | |
| Operating free-air temperature, $T_A$ | RC4558 | 0 | 70 | °C |
| | RM4558 | ±55 | 125 | |

# 5. INTERNAL BLOCK DIAGRAM OF ICS

## Pt2558

### APPLICATION CIRCUIT




### ORDER INFORMATION

| Valid Part Number | Package Type |
|---|---|
| PT2258 | 20 Pins, DIP Package (300 mil) |
| PT2258-S | 20 Pins, SO Package (300 mil) |

# 5. INTERNAL BLOCK DIAGRAM OF ICS

## Pt2558

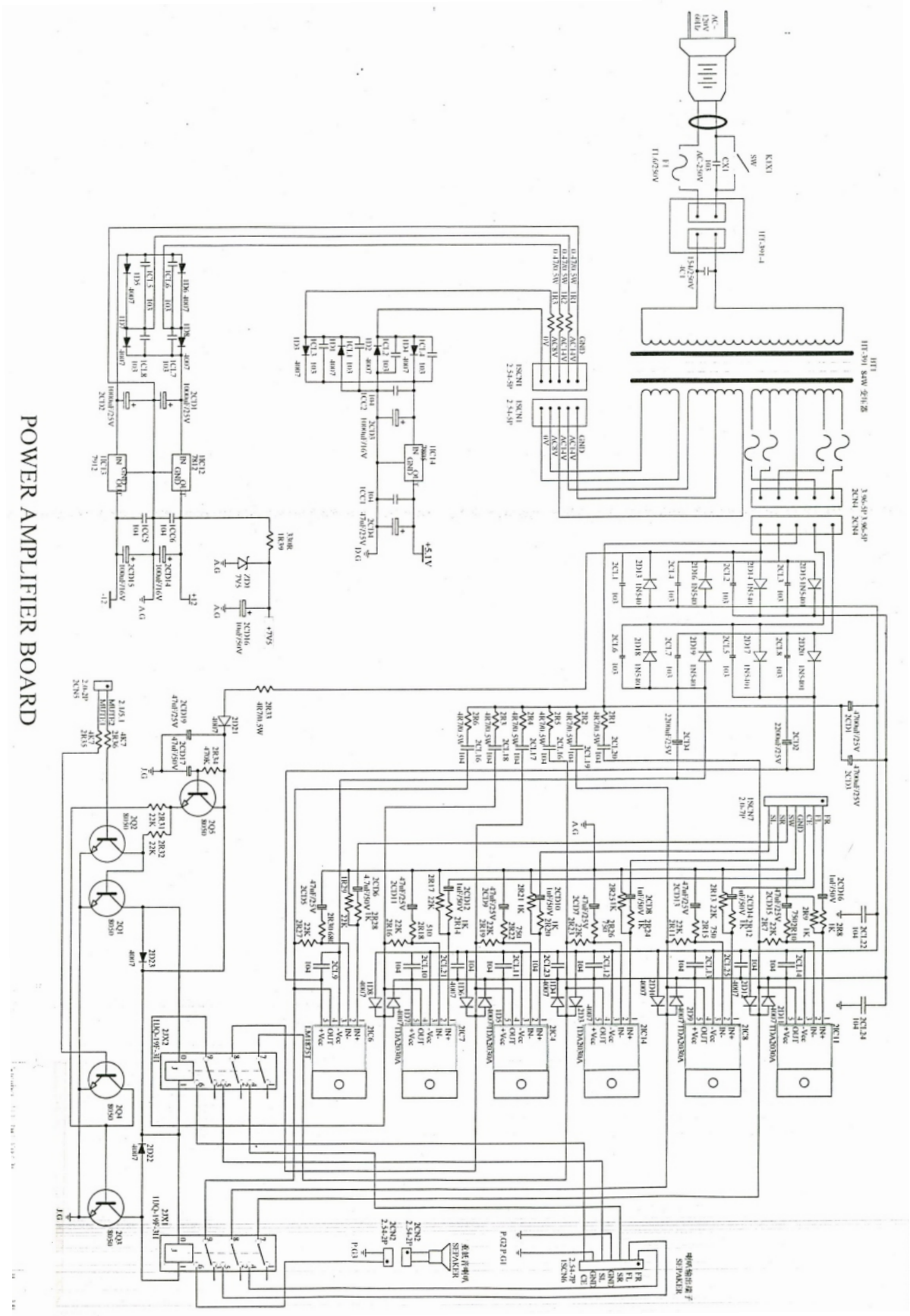
### ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD | Supply Voltage | | 5 | 9 | 10 | V |
| Is | Supply Current | | | 8 | | mA |
| RIN | Input Impedance | FL,FR,CTR SUB,SL,SR | 27 | 30 | 35 | KΩ |
| VCL | Maximum Input Voltage | Volume=0dB THD=1% | | 2.8 | 3.0 | Vrms |
| Sc | Channel Separation | | 90 | 100 | 110 | dB |
| CRANGE | Volume Control Range | | | 79 | | dB |
| AVMAX | Maximum Attenuation | | | -79 | | dB |
| Astep | Attenuation Step | | | 1 | | dB |
| EA | Attenuation Error | Volume=0~-50dB | -1.0 | 0 | +1.0 | dB |
| AMUTE | Mute Attenuation | A-weighting | 90 | 95 | 98 | dB |
| THD | Total Harmonic Distortion | Volume=0dB Input,200mVrms | 0.003 | 0.005 | 0.01 | % |
| Noise | Output Noise | A-weighting | | 3 | 5 | μV |
| S/N | Signal-to-Noise Ratio | 0dB=1Vrms A-weighting | 100 | 105 | 110 | dB |
| Ro | Output Impedance | | | 600 | 900 | Ω |
| Go | Output Gain | | -0.5 | 0 | +0.5 | dB |
| Vomax | Maximum Output | FL,FR,CENTER SUB,SL,SR THD=1% | 2.3 | 2.6 | 2.9 | Vrms |

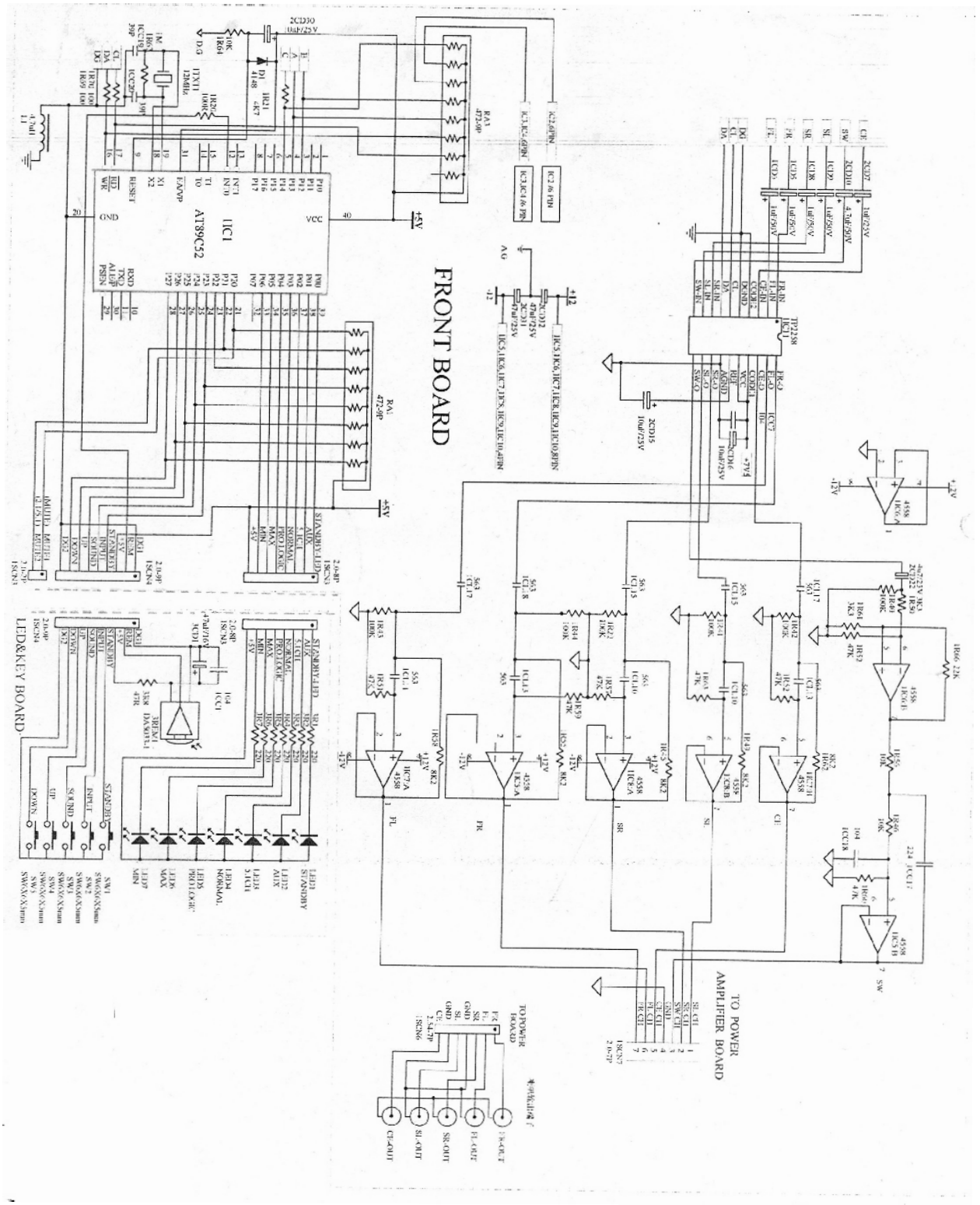
### I²C BUS SECTION ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VIL | Bus Low Input Level | | | 2.4 | 2.5 | V |
| VIH | Bus High Input Level | | 2.8 | 3.0 | | V |
| TINIT | Bus Initialization | Cref=10μF | | 250 | 300 | mS |

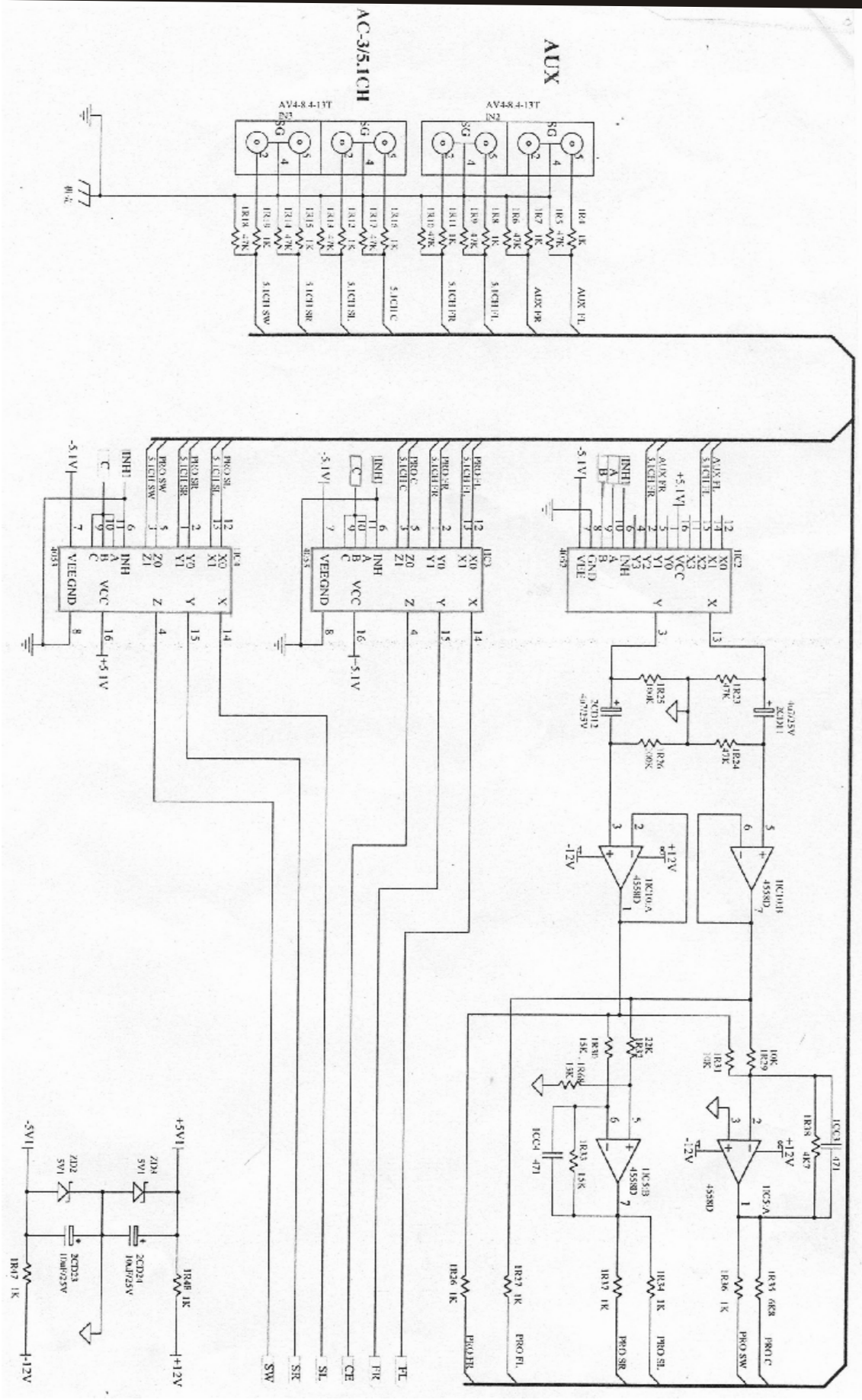
## 6. SCHEMATIC DIAGRAM



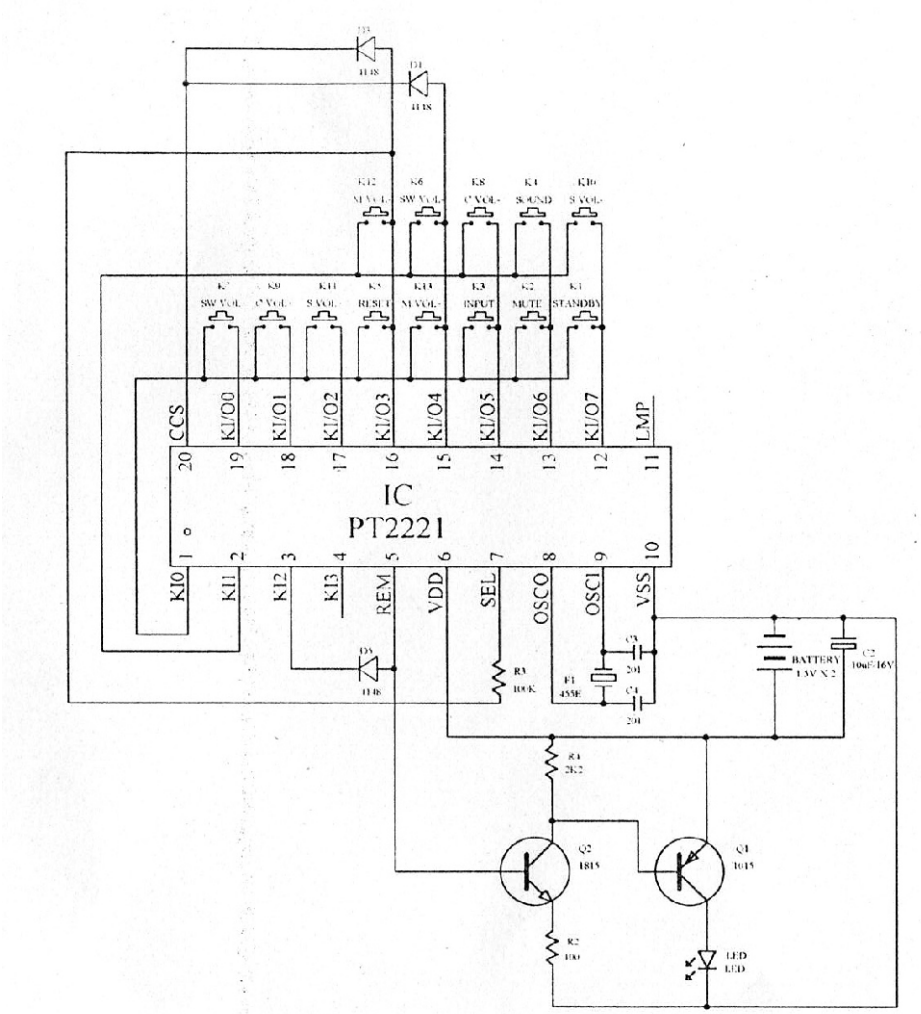
# 6. SCHEMATIC DIAGRAM



# 6. SCHEMATIC DIAGRAM



## 6. SCHEMATIC DIAGRAM




REMOTE CONTROL BOARD